IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 7, 9 and 15 and AMEND claims 1-3, 8, 10, 13, 14 and 16 in accordance with the following:

1. (Currently Amended) A packet transfer device comprising:

a plurality of input/output ports;

a header information extracting circuit for extracting header information belonging to a ~~3rd~~ third layer and a higher ~~layers~~ layer of a network protocol from a ~~packets~~ packet inputted from the respective input/output ports;

a table storing header information and control information corresponding to the header information in association with each other;

a control information acquiring circuit for acquiring the control information corresponding to the header information extracted by said header information extracting circuit from the table; ~~and~~

a processing circuit for processing packets based on the control information acquired by said control information acquiring circuit; and

a process determining circuit for determining a process to be actually performed by said processing circuit if the control information is acquired from a plurality of tables with respect to one packet by said control information acquiring circuit;

where the control information represents either one of said input/output ports from which the packet is output, and said process determining circuit outputs the packet from the input/output port represented by the control information acquired from the table containing header information belonging to the higher layer.

2. (Currently Amended) A packet transfer device according to claim 1, wherein said control information represents whether a filtering process is to be effected on ~~a~~ the packet or not, and said processing circuit discards the packet if said control information indicates that the filtering process is to be effected on the packet.

3. (Currently Amended) A packet transfer device according to claim 2, further comprising an input/output port connected to an external network, wherein said processing circuit filters ~~a~~ the packet inputted from the input/output port connected to the external network if the packet has address information of an internal unit thereof.

4. (Original) A packet transfer device according to claim 1, wherein said control information represents either one of said input/output ports from which to output the packet, and said processing circuit outputs the packet from the input/output port represented by said control information.

5. (Original) A packet transfer device according to claim 1, wherein said table stores a plurality of items of header information belonging to different layers and control information corresponding to the items of header information.

6. (Original) A packet transfer device according to claim 1, further comprising a plurality of tables storing different items of information.

7. (Cancelled).

8. (Currently Amended) A packet transfer device according to claim [[7]]1, wherein said control information represents whether a filtering process is to be effected on ~~a~~ the packet or not, and said process determining circuit discards the packet if the items of control information are acquired from said tables and either one of the acquired items of control information indicates that the filtering process is to be effected on the packet.

9. (Cancelled).

10. (Currently Amended) A packet transfer device according to claim [[7]]1, wherein said control information includes information representing either one of said input/output ports from which to output the packet and information representing whether a filtering process is to be effected on ~~a~~ the packet or not, and said process determining circuit discards the packet if both the information representing either one of said input/output ports from which to output the packet and the information representing whether the filtering process is to be effected on the packet or not are acquired from said tables.

11. (Original) A packet transfer device according to claim 1, further comprising a routing processing circuit for performing a routing process.

12. (Original) A packet transfer device according to claim 1, further comprising a table rewriting circuit for rewriting the information stored in said table.

13. (Currently Amended) A packet transfer device according to claim 1, wherein said control information represents ~~the~~ a priority of ~~a~~ the packet, and said processing circuit processes the packet according to the priority represented by said control information.

14. (Currently Amended) A packet transfer device according to claim [[1]]13, further comprising a storage circuit for temporarily storing ~~a~~ the packet, wherein said processing circuit writes, reads, and transmits the packet stored in said storage circuit based on the priority ~~thereof~~ of the packet.

15. (Cancelled).

16. (Currently Amended) A packet transfer system for transferring packets between a plurality of networks connected by a packet transfer device, said packet transfer device comprising:

a plurality of input/output ports;

a header information extracting circuit for extracting header information belonging to a ~~3rd~~ third layer and a higher ~~layers~~ layer of a network protocol from packets inputted from the respective input/output ports;

a table storing header information and control information corresponding to the header information in association with each other;

a control information acquiring circuit for acquiring the control information corresponding to the header information extracted by said header information extracting circuit from the table; ~~and~~

a processing circuit for processing packets based on the control information acquired by said control information acquiring circuit; and

a process determining circuit for determining a process to be actually performed by said processing circuit if the control information is acquired from a plurality of tables with respect to one of the packets by said control information acquiring circuit;

where the control information represents either one of said plurality of input/output ports from which the packets are outputted, and said process determining circuit outputs the packets from one of said plurality of input/output ports represented by the control information acquired from the table containing header information belonging to the higher layer.